



Research Consortium in Speckled Computing

# A Low-Power Digital Transceiver for the 5Cube

Neil MacEwen & Louise Crockett

University of Strathclyde

[specknet@eee.strath.ac.uk](mailto:specknet@eee.strath.ac.uk)



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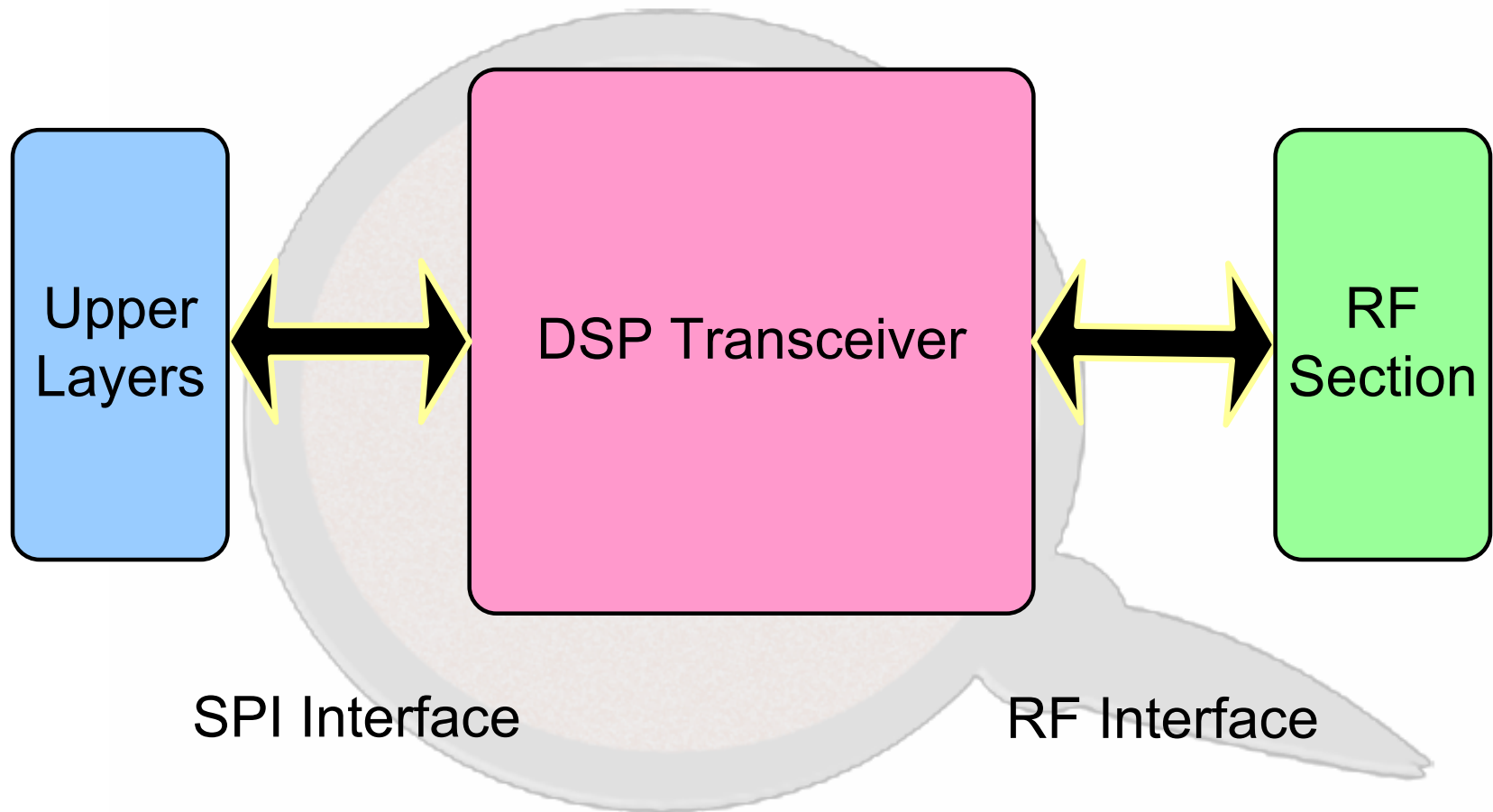


# Outline

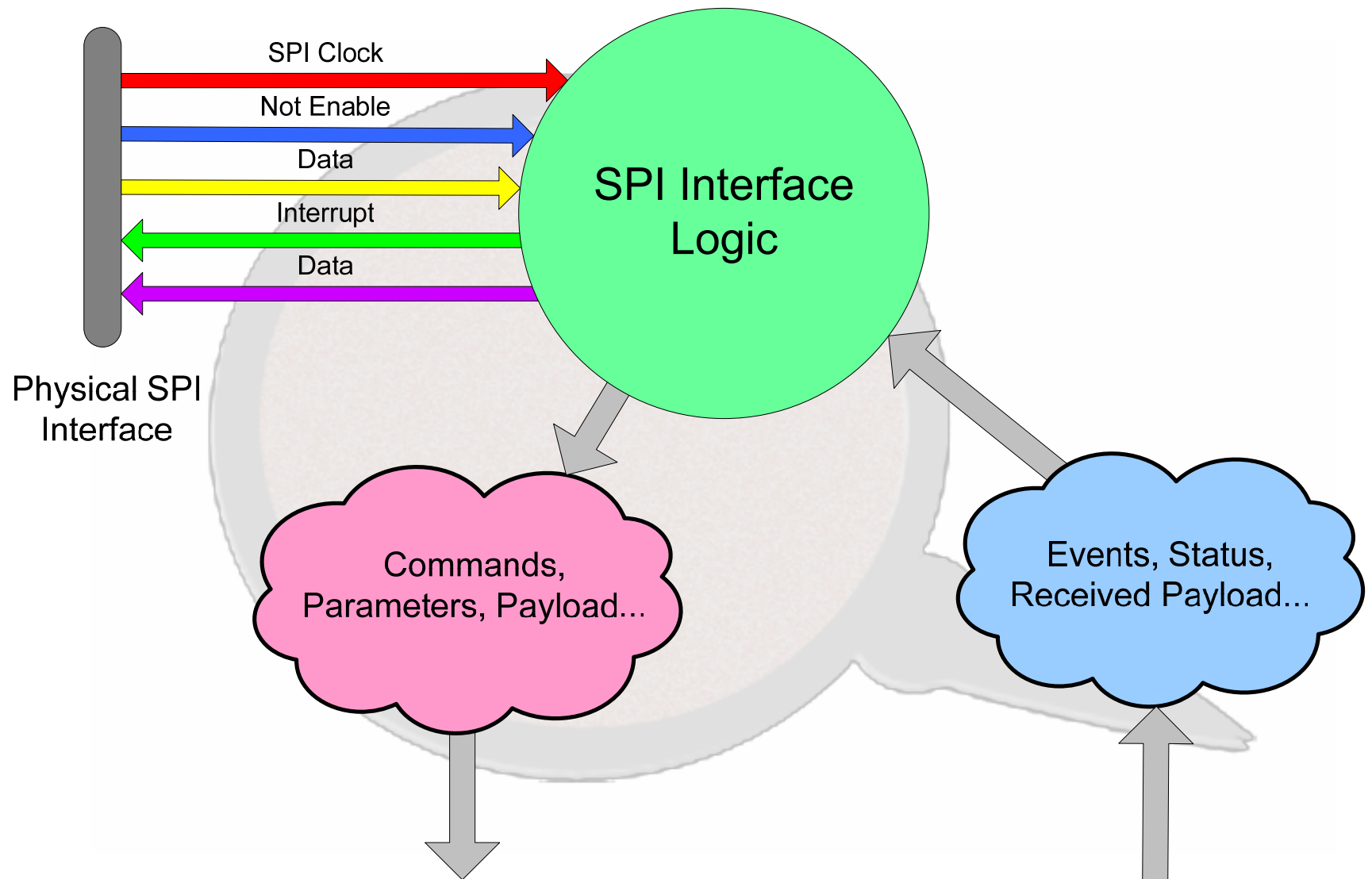
- 5Cube Transceiver
  - 1<sup>st</sup> generation implementation
  - Interfacing
  - Control
- DSP Physical Layer
  - Reducing the synchronisation overhead
  - Using a primitive clock
  - Pulse shaping
- The future
- Conclusions

- First generation speck
  - Off-the-shelf microprocessor
  - Custom designed physical layer
    - DSP on ASIC, RF circuitry on MMIC
  - Commercial battery
    - Power output limited by volume
- Low power and low complexity 1<sup>st</sup> priority

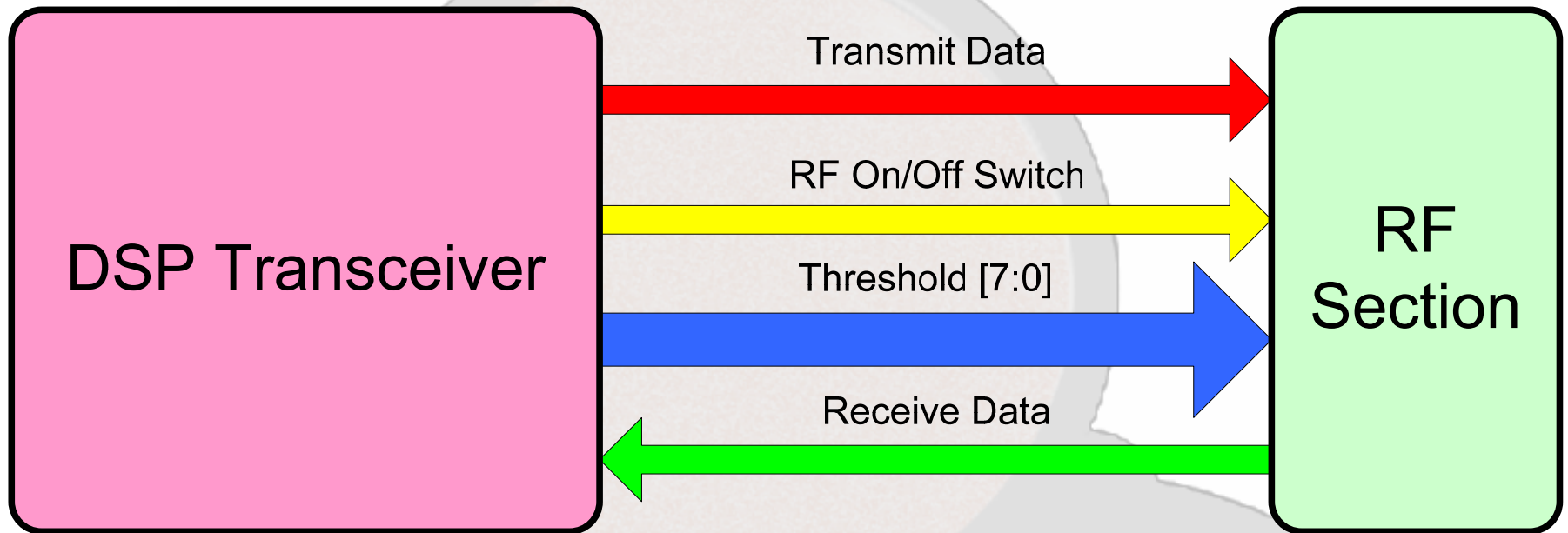
# 5cube block diagram



# SPI interface

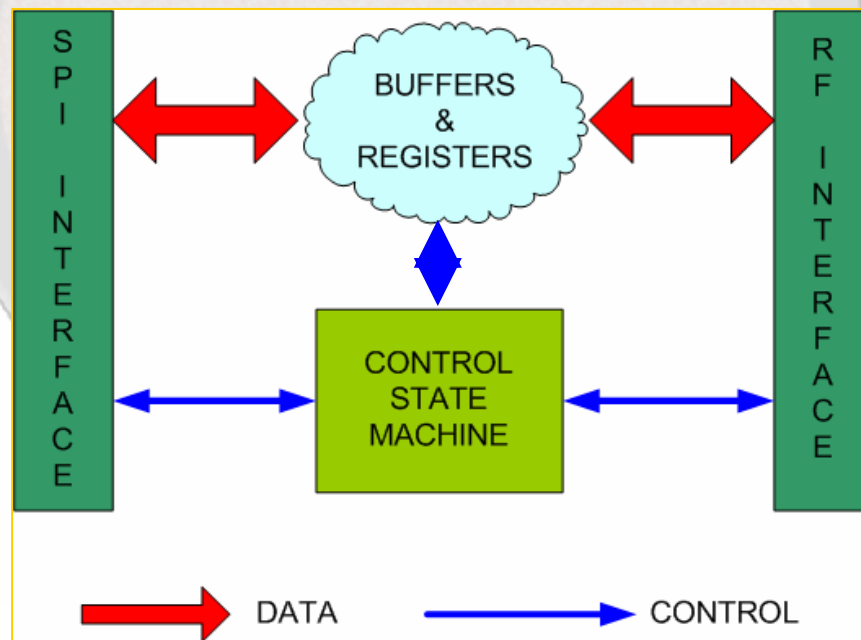


# RF interface

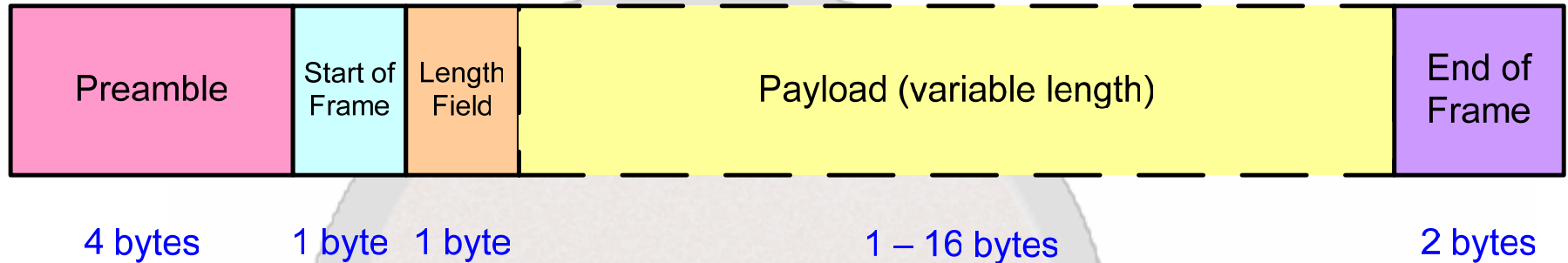


# Control/buffers/fsm

- State machine acts on and replies to commands from SPI interface
  - Loads and reads from storage, controls transmission and reception of packets, turns RF on/off
- Various buffers and registers store information
  - Transmit and receive payload, status, threshold etc



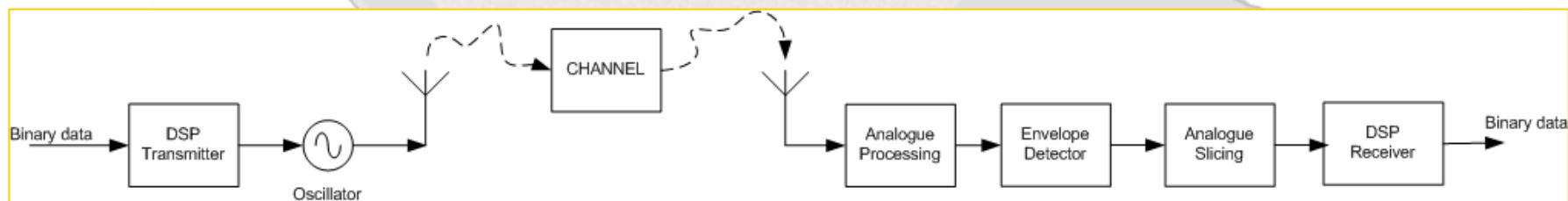
# Packet Format



- Preamble length to be evaluated
- Payload is 1-16 bytes at present but will grow
- End of Frame may be used to check packet length

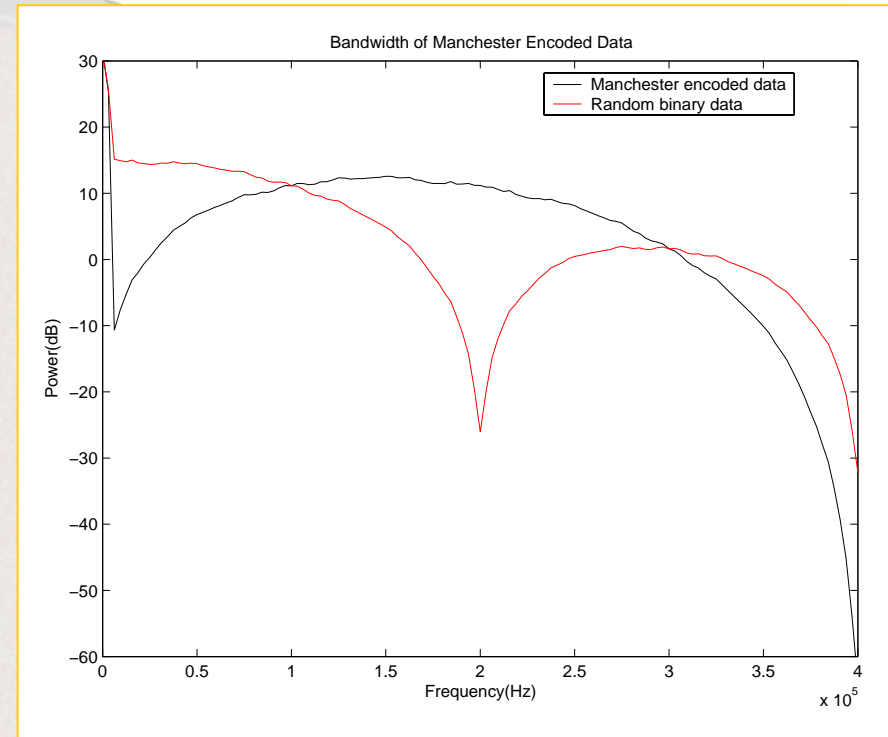
# Low-Power RF Communications

- OOK modulation & envelope detection
  - No active components in receiver
- Analogue slicing
- Digital transceiver
  - Baseband modem
  - Frame and symbol synchronisation
  - Control and interfacing circuitry

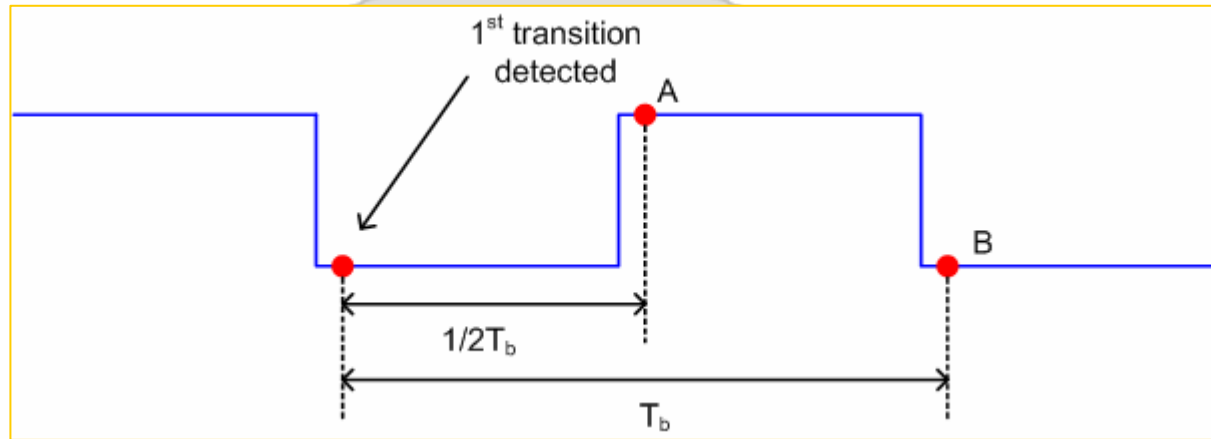


# Reducing The Synchronisation Overhead

- Simplification – transmit clock in data
  - Manchester encoding
    - Transition within each bit period
  - Trade bandwidth for simplicity
- Manchester decoder
  - Transition detector and counter



# Using a primitive clock



- Decoder tolerant to a range of oversampling ratios

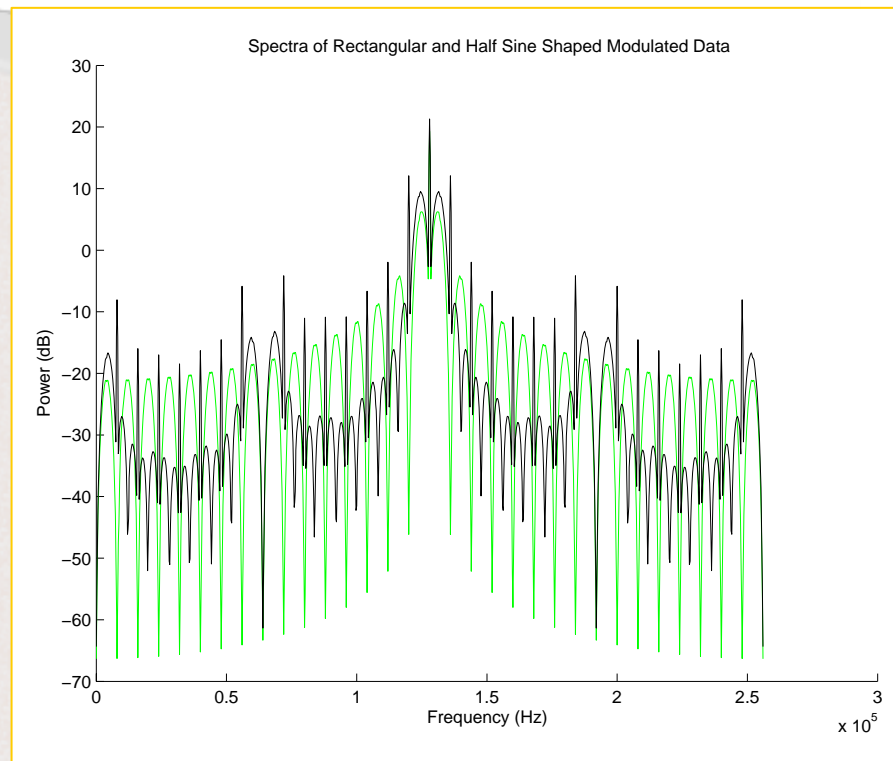
$$\delta \leq \frac{OSR - N}{OSR + N}$$

$$OSR = 8 \quad \Rightarrow \quad \delta = \mathbf{14.29} \%$$
$$N = 6$$

- An **inaccurate, low-cost and low-power** clock

# Pulse Shaping

- On Off Keying with Rectangular Pulse Shaping
  - Allows most of the signal energy to escape!
    - Only 23% remains in the band of interest
- Half Sine performance:
  - Signal better concentrated in band of interest
    - Increased from 23% to 45%
  - ~300 gates



# The future – adding functionality

- Error correcting/detecting codes
- Configurable packet formats
- Slicing
  - Bring into DSP
  - Automatic Gain Control (AGC) / ADC
- Enhanced SPI interface
  - More commands
  - Increased status information
- Medium access – channel clear detection
- Duty cycling
- Optical communications
- ASIC design expertise

# The future - research

- Pulse Shaping
  - Increase efficiency/decrease transmit power
  - Compatible with Manchester transceiver?
- Synchronisation
  - Try other implementations
    - How do they compare with Manchester solution?

# Conclusions

- 5Cube first iteration is under way
- DSP transceiver ~11000 gates
  - SPI and RF interfacing
  - Control logic
  - Manchester transceiver
- Plenty of work still to be done
- Learn about ASIC design process
- Start including optics

# Summary

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  - 1<sup>st</sup> generation implementation
  - Interfacing
  - Control
- DSP Physical Layer
  - Reducing the synchronisation overhead
  - Using a primitive clock
  - Pulse shaping
- The future
  - Adding functionality
  - research
- Conclusions