

Low Arithmetic Complexity QPSK IF Radio Implementation

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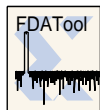


Outline

- QPSK IF transceiver design
 - Objective, Specialization, System parameters
- Transmitter structure
- Transmitter details
- Receiver structure
- Receiver details
- Simulation results
- Ongoing carrier synchronizer
- Future work

QPSK IF Transceiver Design

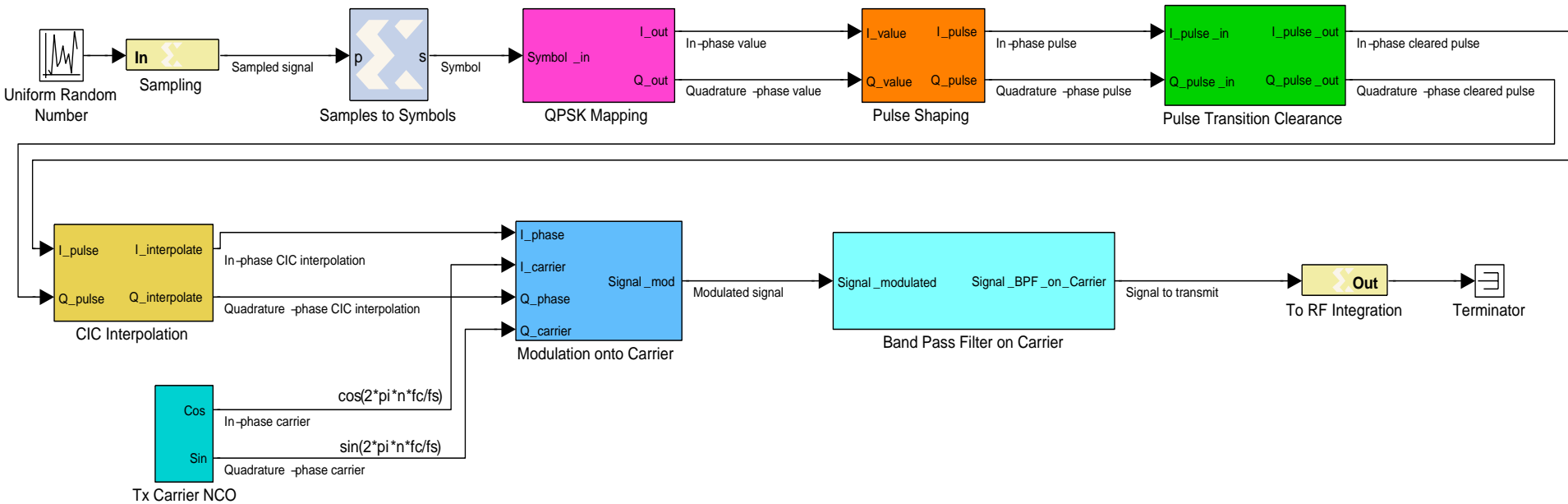
- Objective: low cost, low power IF with acceptable performance for SpeckNet
- Quaternary Phase Shift Keying (QPSK) chosen as modulation scheme, for high bandwidth efficiency purpose
- Root raised-cosine (RRC) filter chosen for pulse shaping, to reduce inter-symbol interference (ISI) with bandwidth constraint
- Cascade integrator comb (CIC) filter used to design interpolator (at Tx) and downconverter (at Rx), to save computing and hardware cost
- Design based on Xilinx System Generator
 - system sampling rate: 16M Hz
- Data rate: 25k sample/sec, 8 bit/sample
- Carrier signal at 1M Hz, can be changed



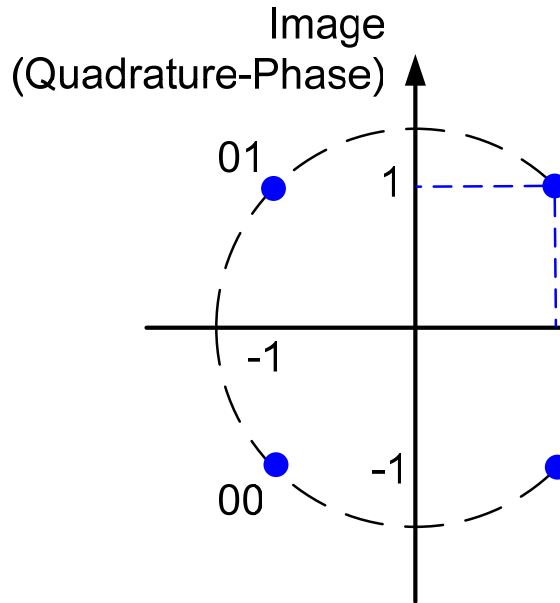
System Generator

RRCpulse

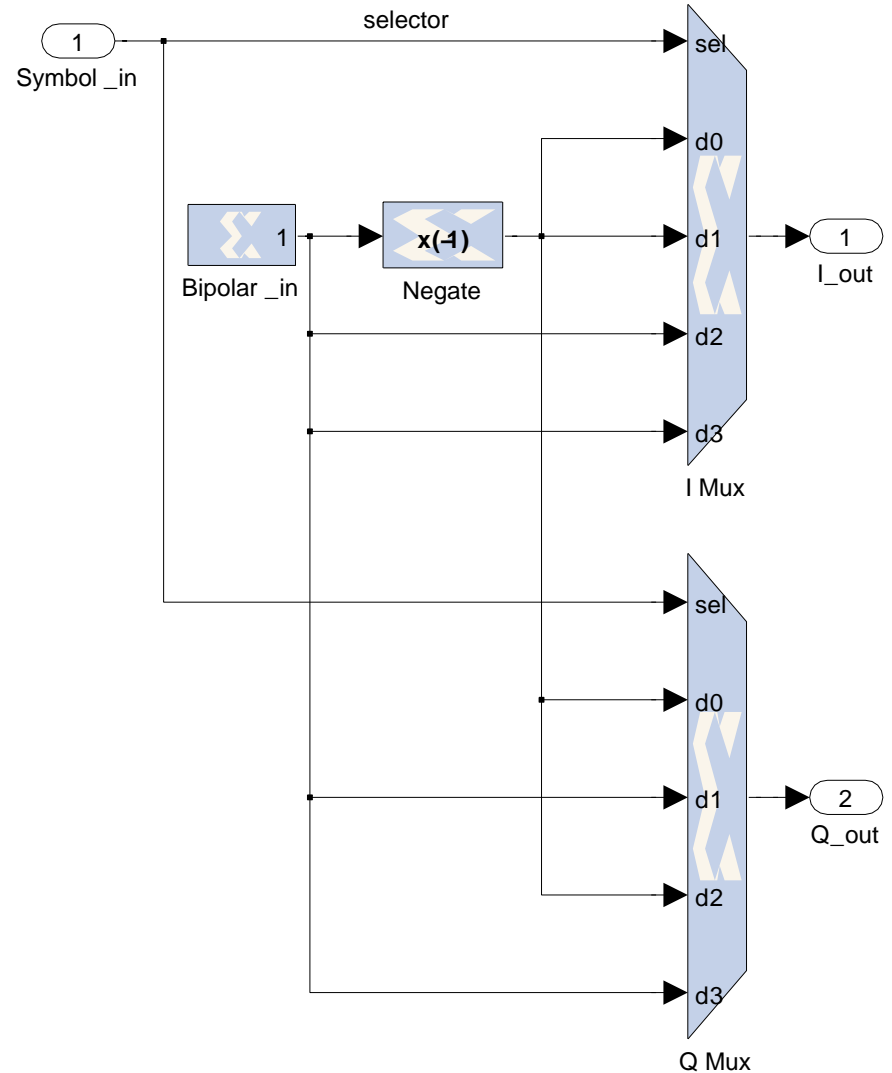
CarrierBPF



Tx - QPSK Mapping

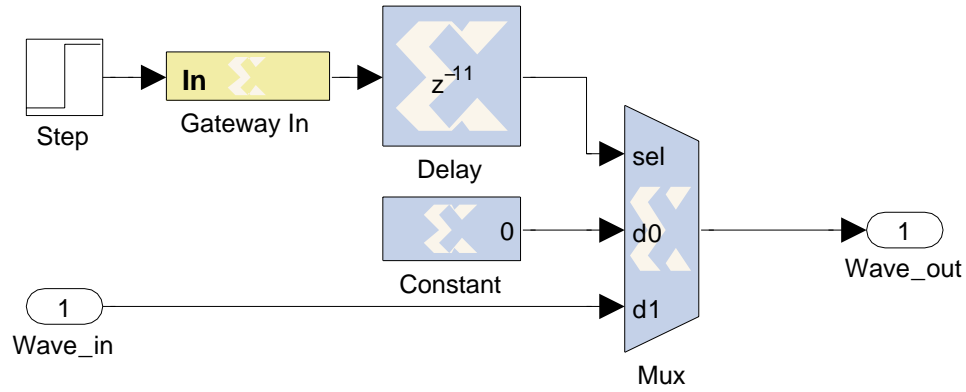
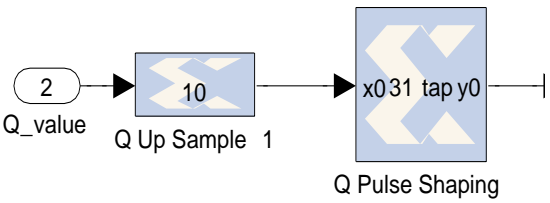
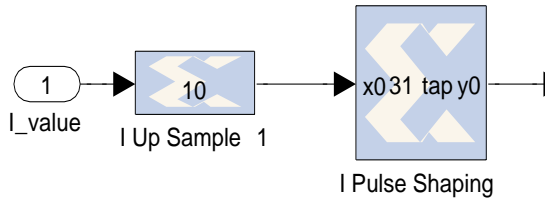


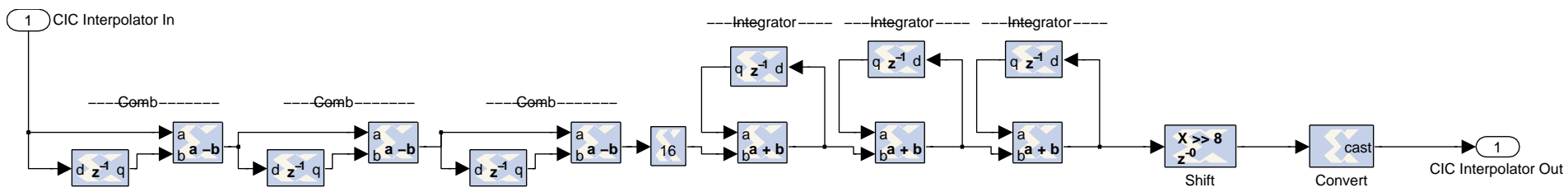
- Signal Space for QPSK Mapping, Gray encoded
- Implemented via 2 multiplexers

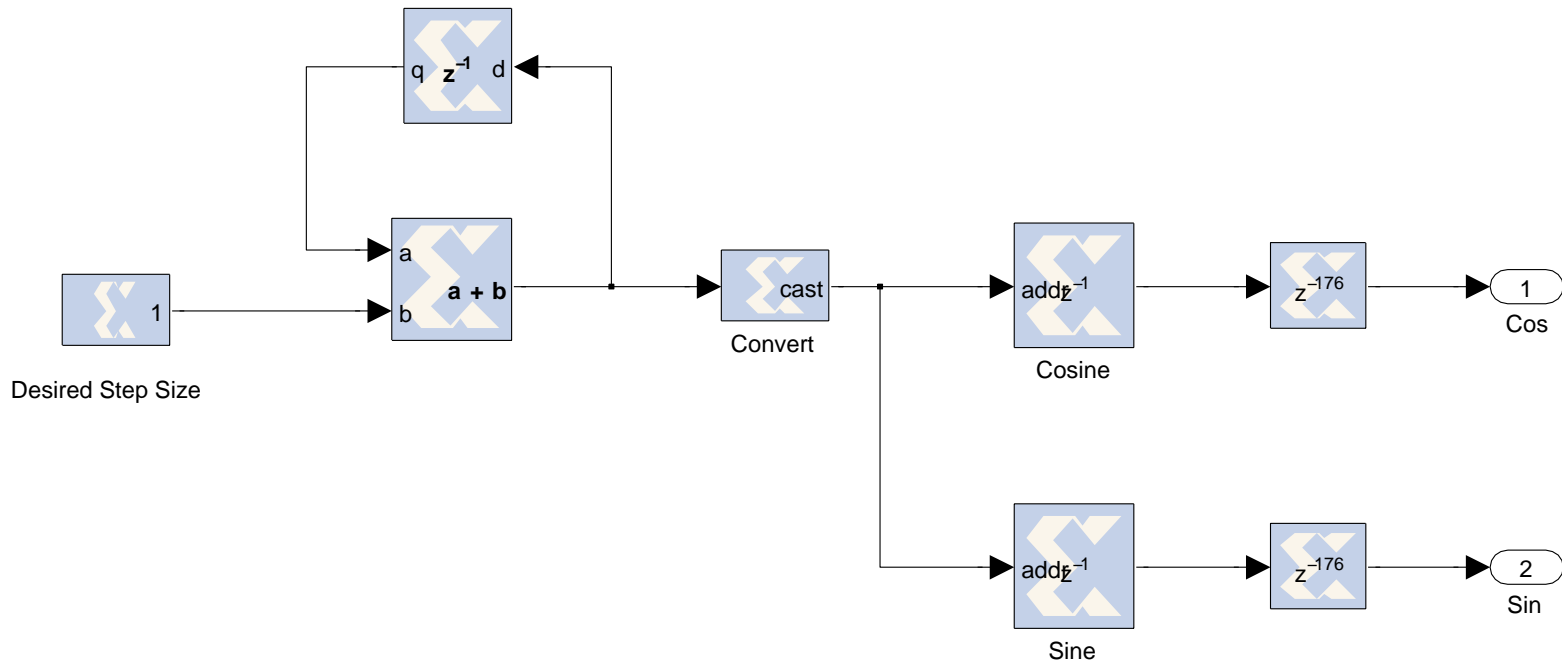


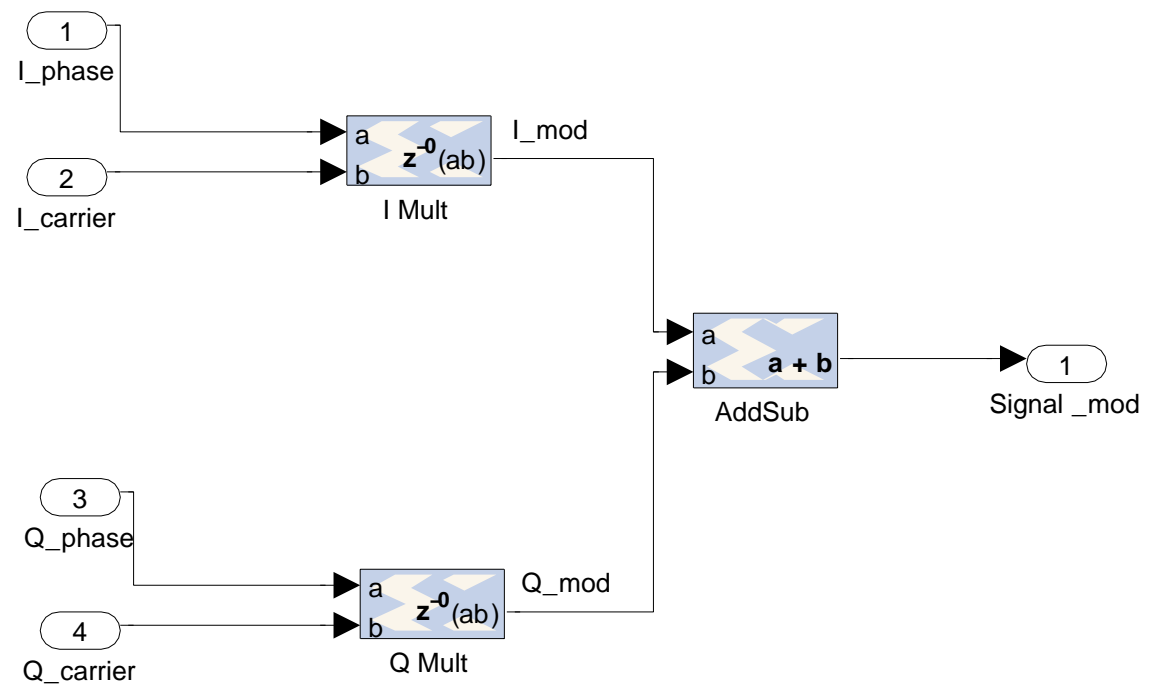


RRCpulse

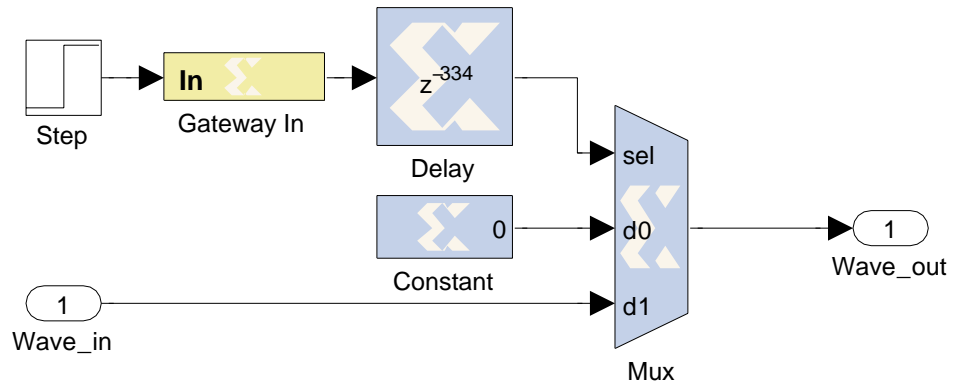








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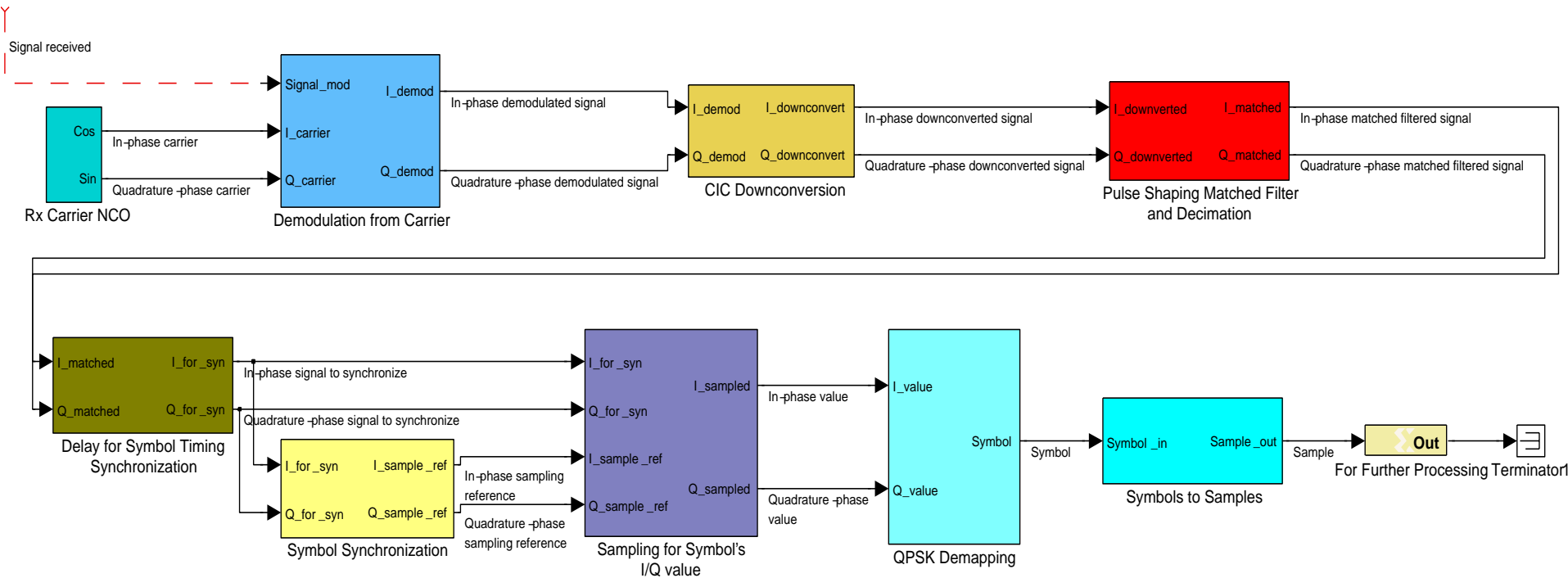


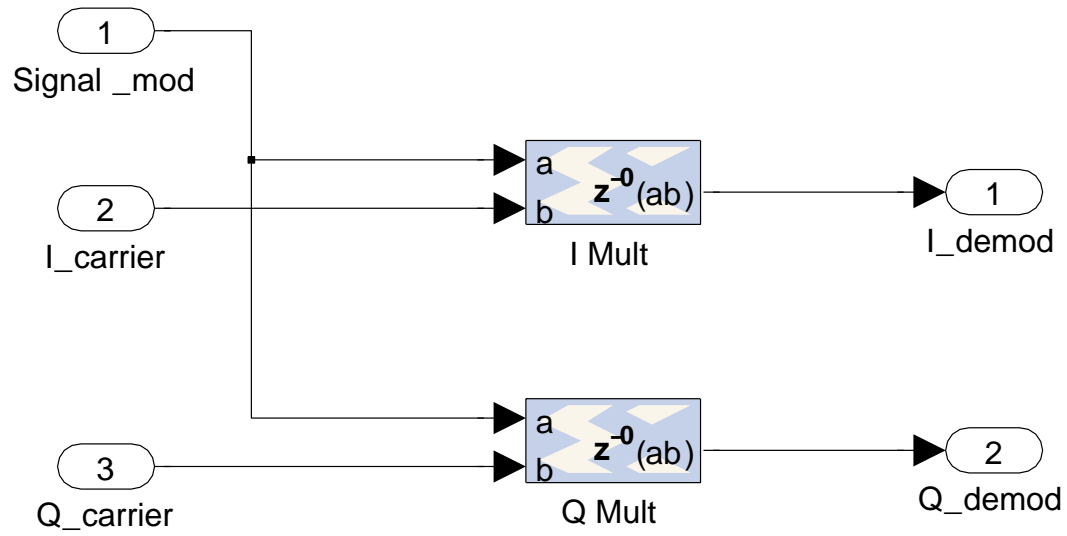


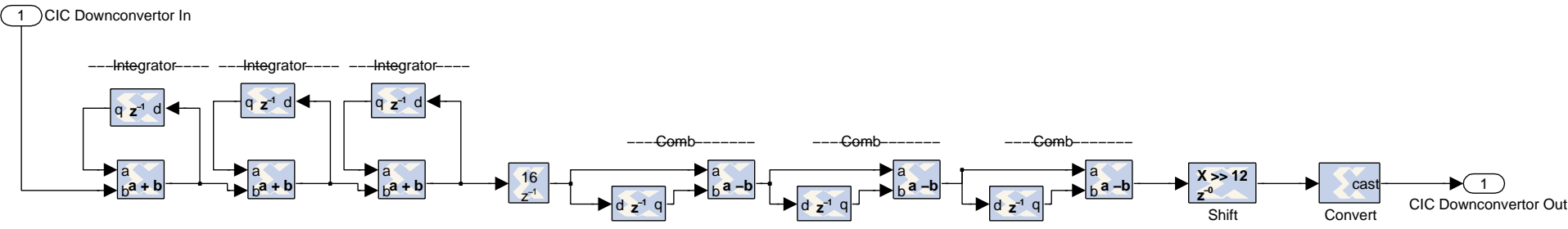
System Generator



EDATool

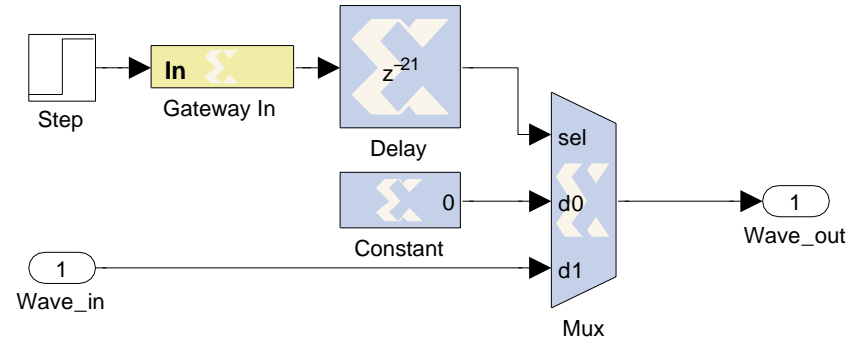
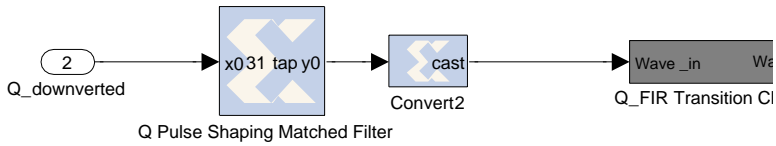
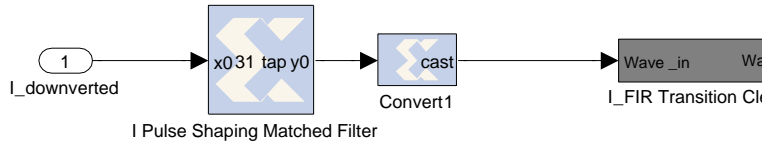




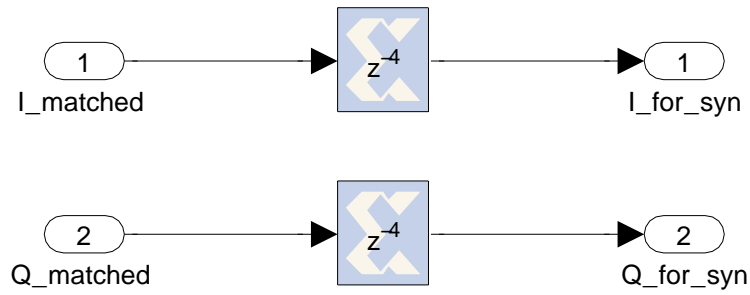
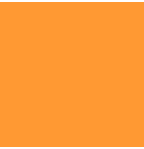




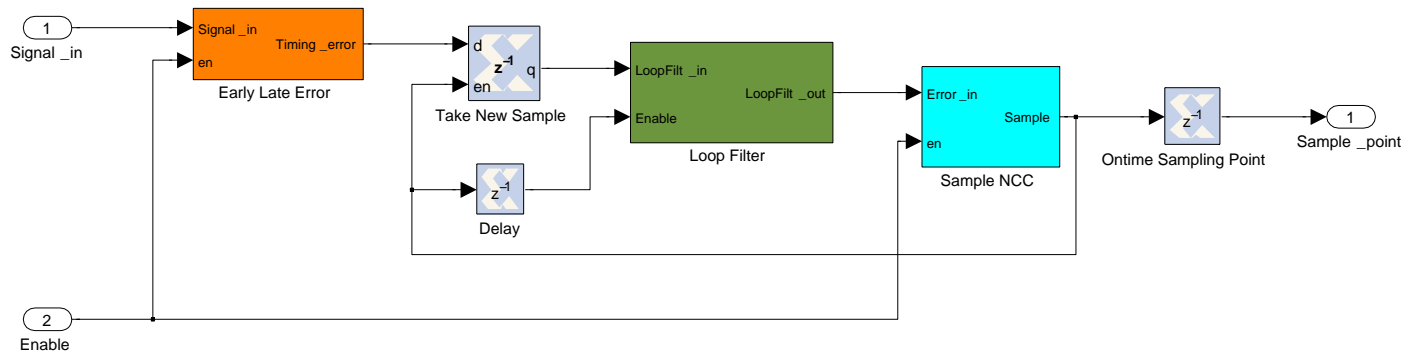
RRCpulse



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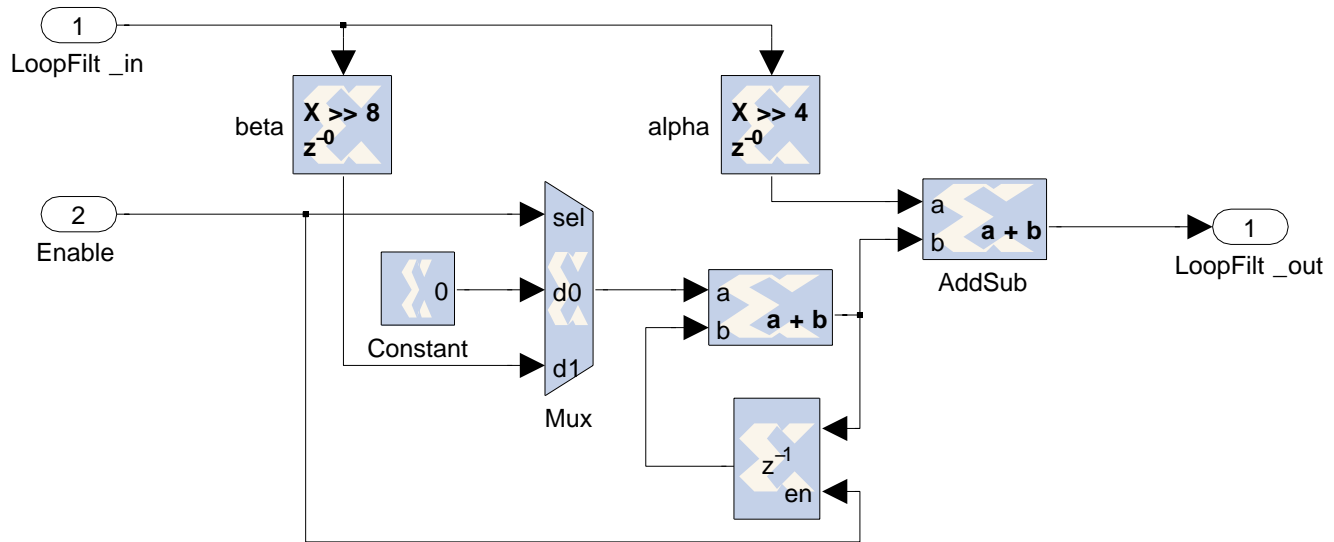


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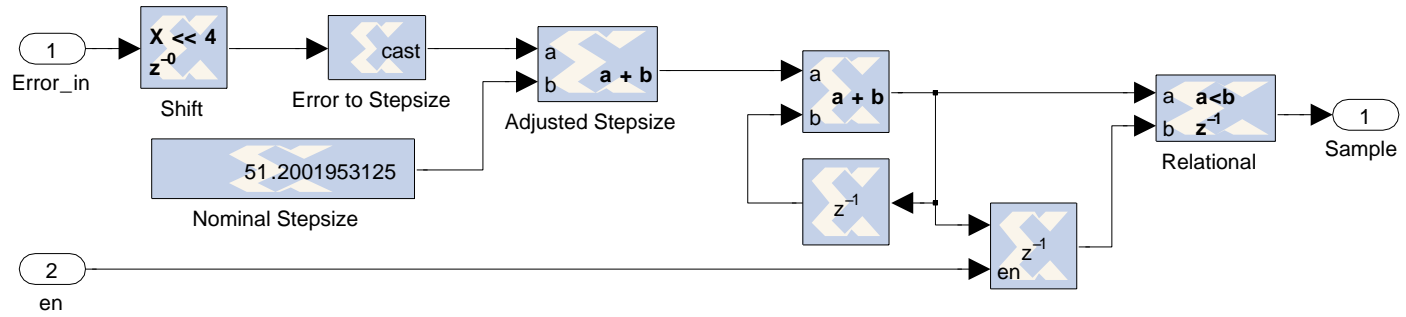
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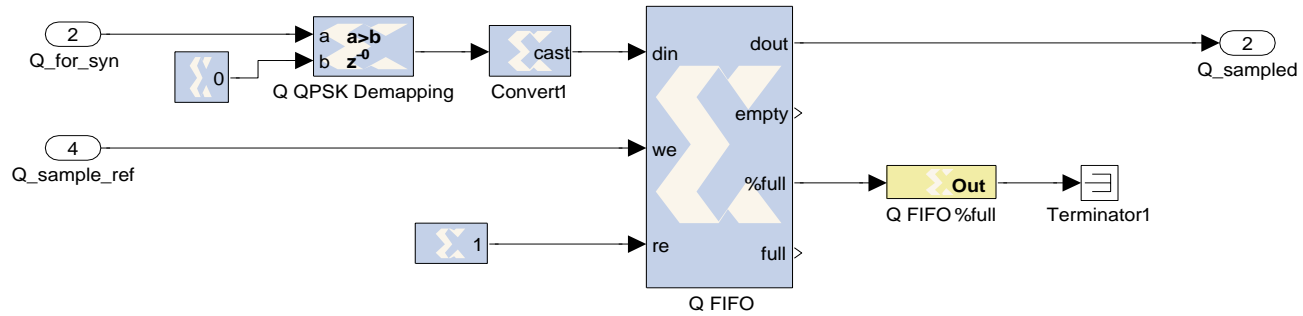
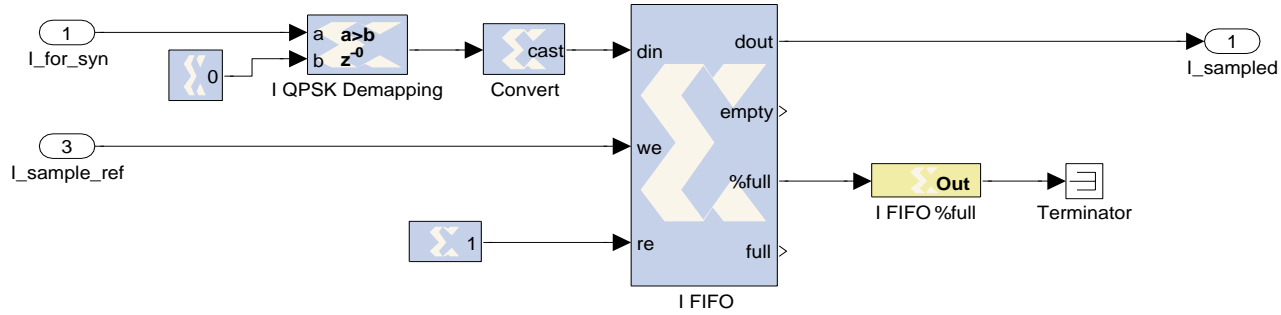
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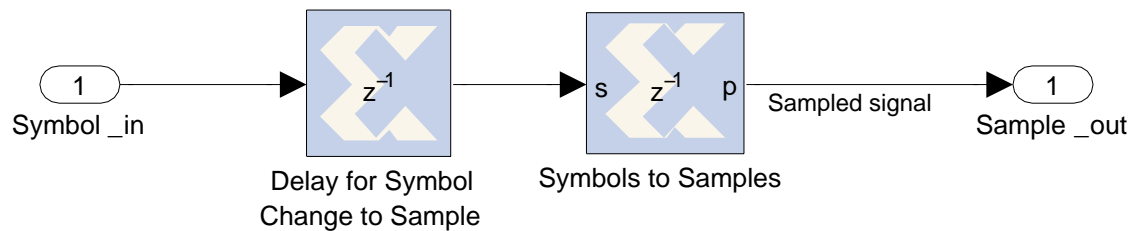
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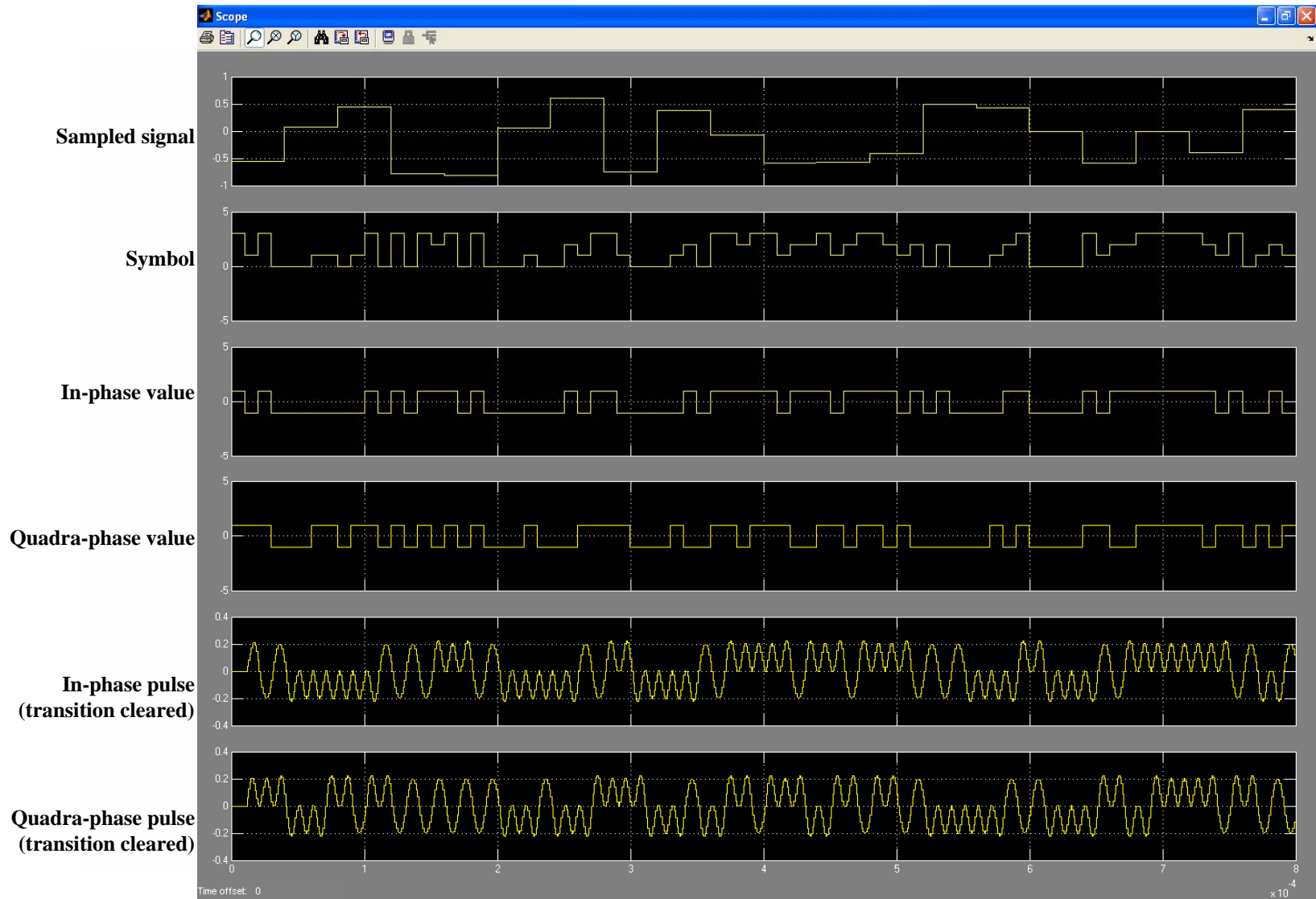
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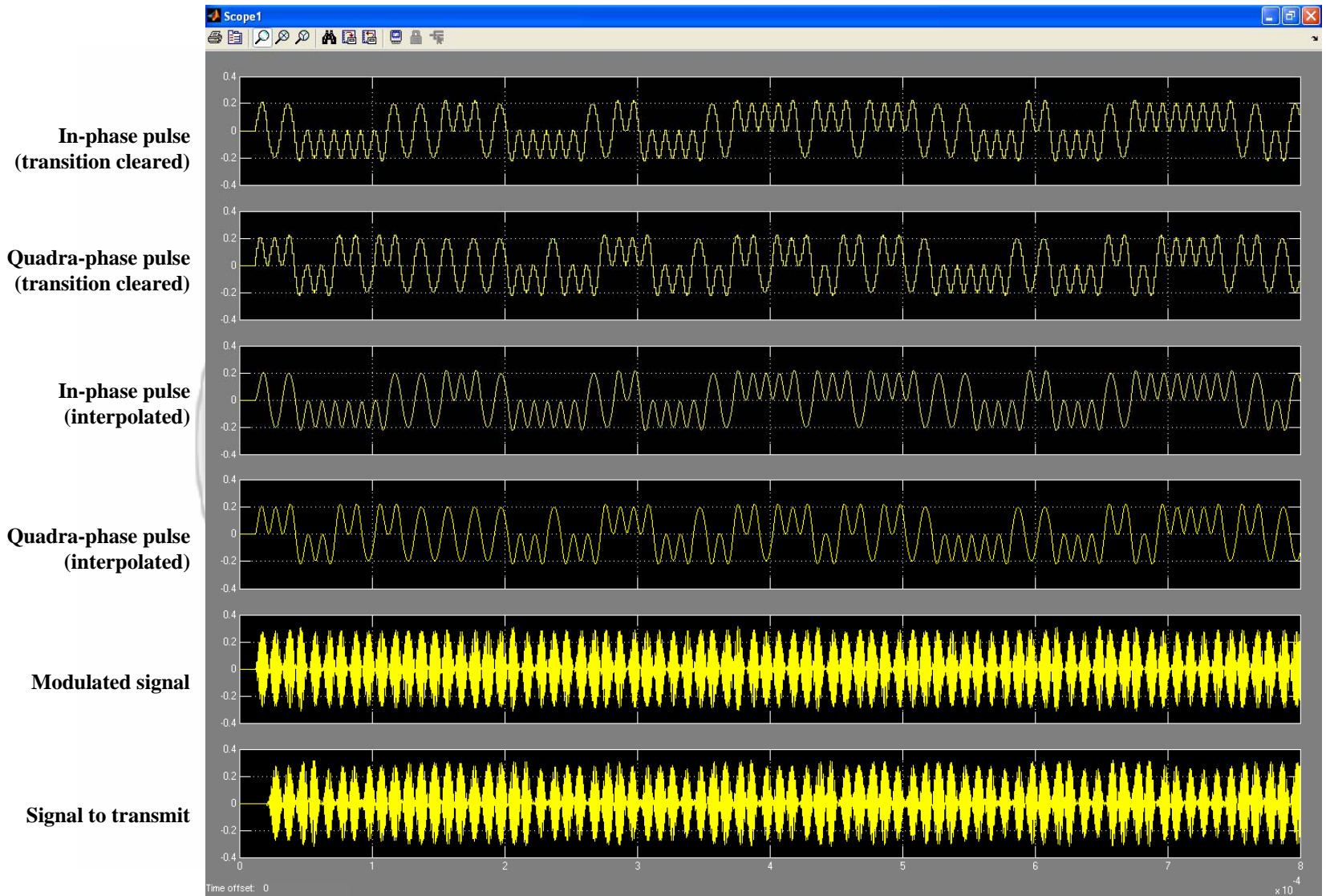


- Change QPSK symbols (2 bit) to original samples (8 bit), using dequantization
- Implemented via 1 delay (to compensate current symbol delay) and 1 serial to parallel block

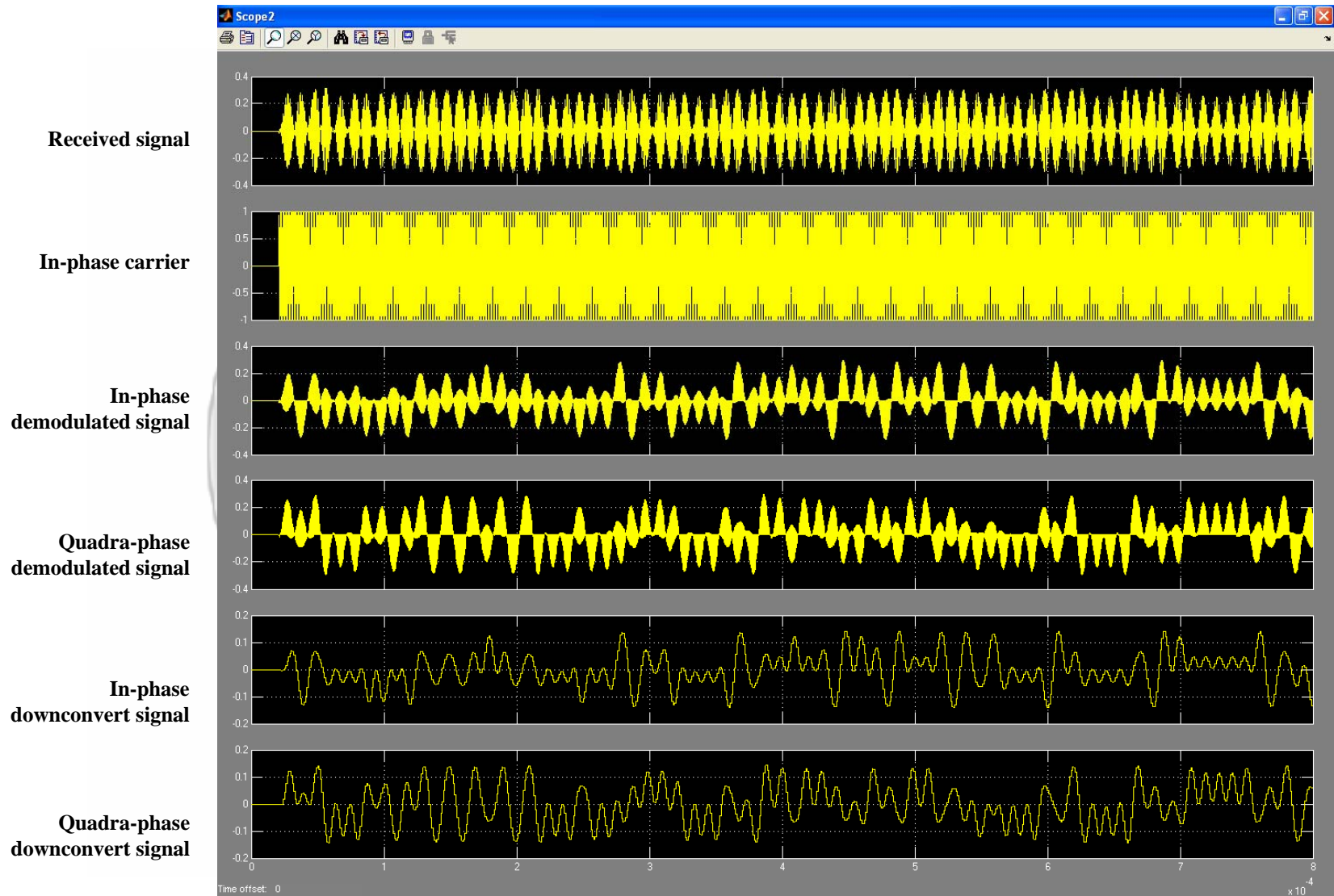
Simulation Results - Tx



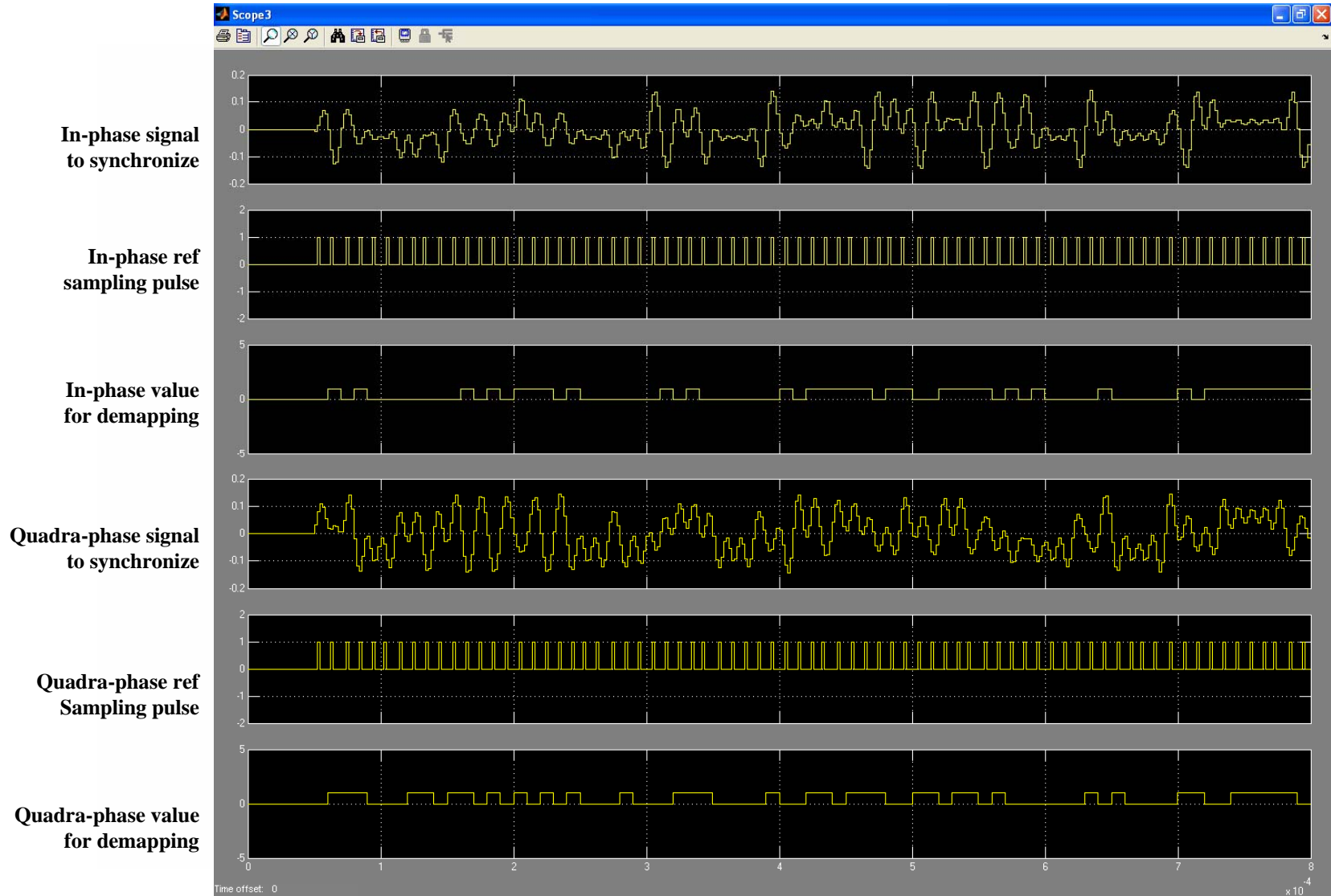
Simulation Results - Tx (cont.)



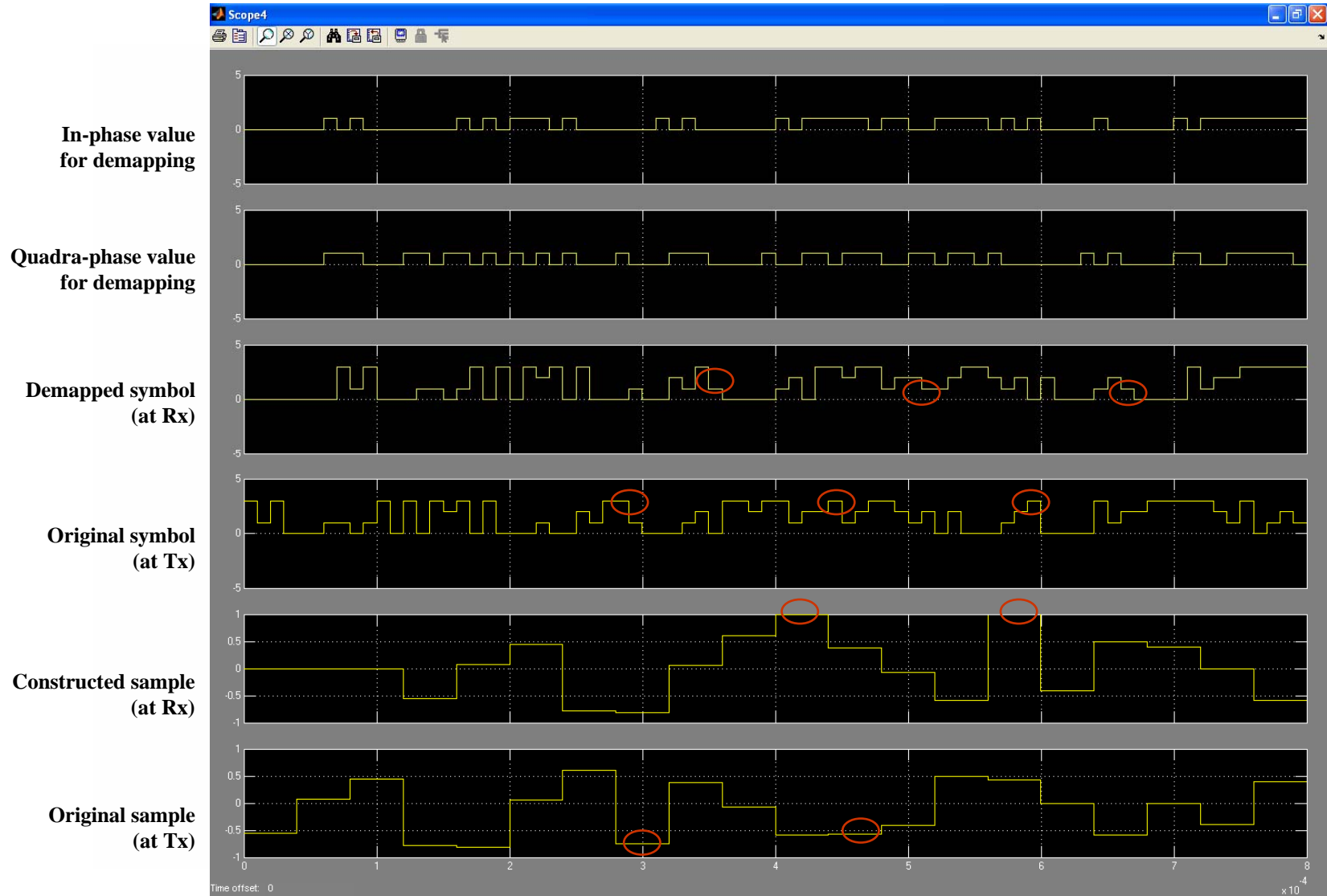
Simulation Results - Rx



Simulation Results - Rx (cont.)



Simulation Results - Rx (cont.)

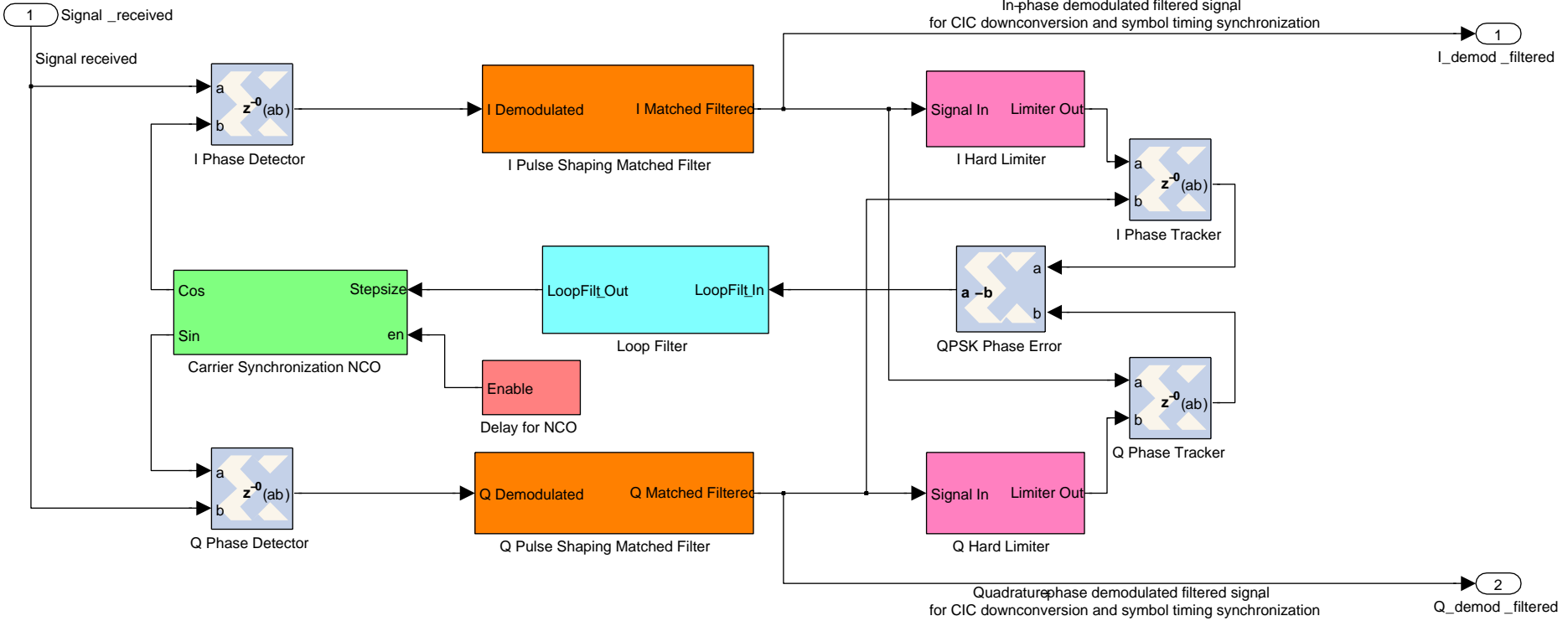


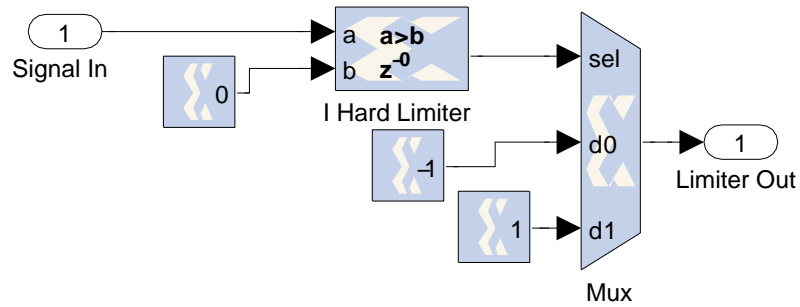
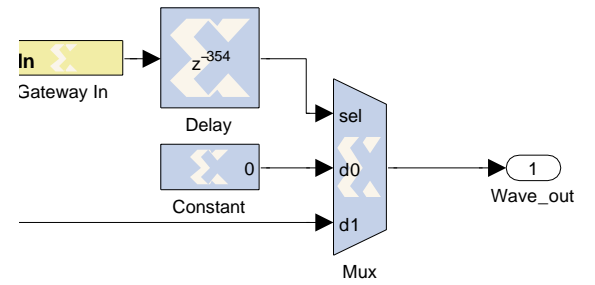


System Generator



RRCPulse

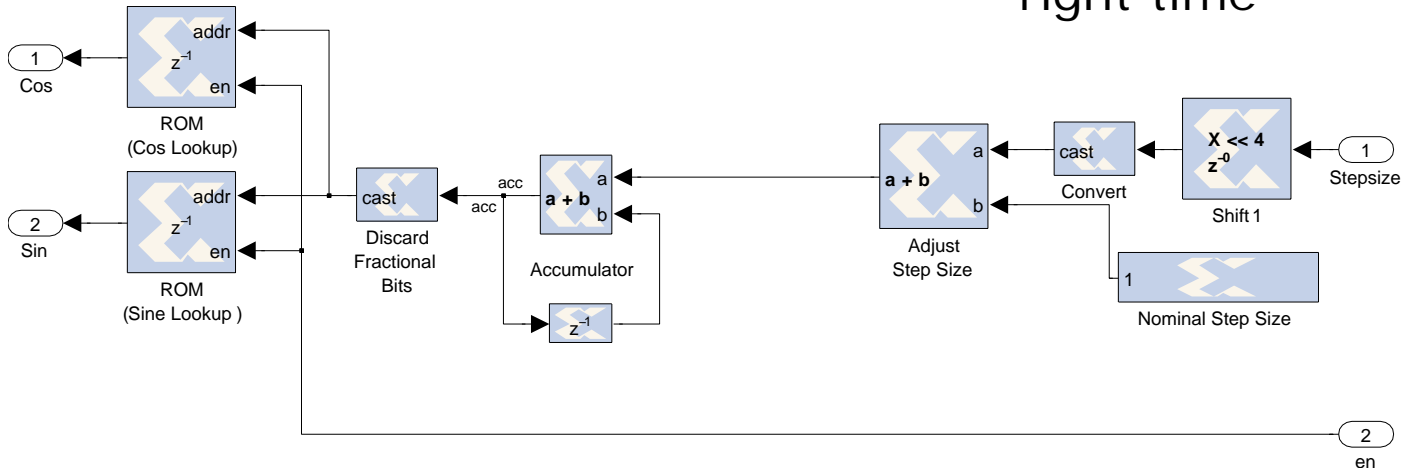




, coefficient

ultiplexer

- Loop filter similar to the one in symbol timing synchronization block
- Numerical controlled oscillator (NCO) consists an adjustable (by phase error) step size to drive accumulator for address in sine wave LUT
- NCO is delayed to let synchronizer start work at right time



Future Work

- Design QPSK carrier recovery part – possible Costas Loop for Differential QPSK (DQPSK) to solve pi ambiguity problem
- Test transceiver in noise environment
- Use reference model to adjust parameters, for performance via computing & hardware cost comparison, to get optimal transceiver setting under a certain cost constraint
 - Adjustable parameters: pulse shaping filter and FIR filter order and coefficient wordlength, LUT depth and output precision, CIC filter order, ...
- Consider sigma-delta structure to save computation and hardware
- Lower cost synchronizer (carrier & symbol)
- Work closely with University of Glasgow for interface with RF section design

The End

Thank you!

Questions?