Symbol Synchronisation Implementation for Low-Power RF Communication in Wireless Sensor Networks

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***Abstract* –Speckled Computing is a novel vision of a wireless sensor network consisting of small nodes which can sense, compute and network wirelessly. The nodes will individually have limited power and processing resources, but together will form a powerful processing system. Electrical power resources at such a volume are severely restricted, and as such design decisions are made with low-power as the first priority. This work examines the use of Manchester encoding in the digital transceiver to reduce the complexity of symbol synchronisation. A Manchester decoder has been implemented which has the useful property of being tolerant to oscillator inaccuracies, allowing a cheap and low-power clock source to be employed. A realistic implementation of the decoder using rectangular pulse-shaping and an oversampling ratio of 8 allows an on-chip oscillator tolerance of more than 11%.**

I. INTRODUCTION

The Speckled Computing Consortium [1] is a collaborative project involving research groups in five universities. The consortium has a vision of ubiquitous computing which will consist of ad-hoc wireless sensor networks of “specks”; tiny, inexpensive 125mm^3 nodes capable of autonomous sensing and processing. Individually the specks will not possess significant computational power; however each speck will be capable of radio frequency (RF) and optical communication, and hundreds or thousands of specks together will form powerful programmable computational networks called SpeckNets.

Fig. 1 shows an overview of the Speckled Computing research interests (reproduced from [2]). Speckled Computing is envisaged as an enabler technology for ubiquitous computing. The future vision is of a SpeckNet which will be scattered, or painted or sprayed onto an object turning that object into an intelligent entity capable of sensing, processing and communication. Various applications are foreseen from stress monitoring on load-bearing equipment such as bridges or aeroplanes to location monitoring and heart-rate supervision.

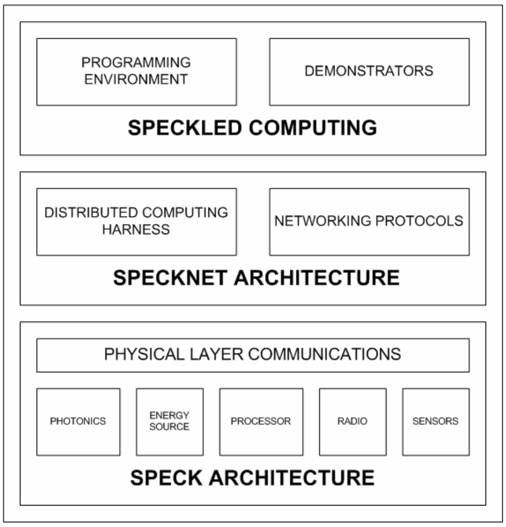

Fig. 1: Overview of Speckled Computing research areas (reproduced from [2]).

A first generation SpeckNet will be developed over the next few years with specks as 125mm^3 nodes capable of RF and optical communication and simple processing using a commercially-available microcontroller [3]. Data rates will initially be limited to a few kbps.

Each speck will contain its own energy source within the stated volume and as such battery volume must be kept to a minimum. At present lithium ion technology provides the highest volumetric energy density [4]. The smallest currently commercially-available battery [5] will be suitable for a first generation speck, but nevertheless a low-power transceiver design is critical to providing a useful lifetime. Minimising power consumption in the design of a speck transceiver, both in terms of hardware and cost of communication, is therefore the crucial factor.

This paper is a study of how Manchester encoding has been used to reduce the complexity of the receiver design, and in particular symbol synchronisation. Section II looks at the design of the transceiver for the first generation speck.

Published in the Proceedings of *The Asilomar Conference on Signals, Systems and Computers, October 30 – November 2 2005, Pacific Grove, CA, USA.*

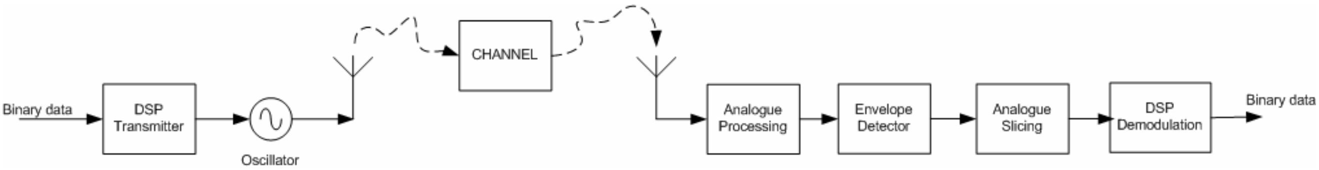

Fig. 2: Block diagram of the basic transceiver used in a first generation speck.

Section III examines the use of Manchester encoding to simplify symbol synchronisation in the speck. Section IV investigates the Manchester decoder in more detail and examines its robustness against clock tolerances. Section V investigates the effects of non-square pulse shaping on the decoder and Section VI presents criteria for oscillator selection before the paper is concluded in Section VII.

II. TRANSCEIVER

Fig. 2 shows a model of the basic transceiver used in the first generation speck. In order for power-consumption to be kept to a minimum an On-Off Keying (OOK) system has been chosen. This results in an extremely simple RF transmitter where the oscillator at the carrier frequency is switched directly by the data to be transmitted. The RF receiver consists of some simple processing such as filtering, an envelope detector and some bit-slicing circuitry. Using an envelope detector for demodulation avoids the use of power-hungry active analogue components such as mixers or phase-locked loops (PLLs) in the receiver.

Once the signal has been demodulated by the envelope detector the present design uses an analogue slicing circuit to recover the bitstream, which is then presented directly to the digital receiver. This avoids the use of a complex analogue-to-digital converter (ADC). The slicer uses hysteresis to ensure that low-level noise is not presented as data to the digital receiver. At present the threshold level used by the slicer is adjusted further up the protocol stack. However some form of automatic gain control (AGC) will be included in future iterations of the design.

III. SYMBOL SYNCHRONISATION BY MANCHESTER ENCODING

The digital receiver must perform symbol synchronisation to extract the data from the received signal. To achieve symbol synchronisation in systems such as Ethernet a frequently used technique is to embed the clock in the transmitted data and extract it at the receiver. Manchester encoding is one such technique. It has not commonly been used in wireless communications due to the fact that it can increase the bandwidth of the transmitted signal. Fig. 3 shows how Manchester encoding causes the bandwidth of the signal to double. This technique however is suitable for use in a SpeckNet due to the low data rates and short ranges (up to 30cm) utilised.

Manchester encoding is a form of bi-phase pulse code modulation which is achieved simply using a logical XOR operation on the clock and the data. Due to the presence of the clock in the transmitted data a transition will occur in the centre of each bit period. A falling edge represents a logic ‘0’ and a rising edge represents a logic ‘1’. The transition can be used to extract the clock signal from the received signal. The extracted clock can henceforth be used as a local clock and thus symbol synchronisation is achieved.

IV. MANCHESTER DECODER

The implemented Manchester decoder consists of a transition detector and a counter which is used to block between-bit transitions. Between-bit transitions occur when two consecutive bits have the same value, as shown in Fig. 4 where two consecutive ‘0’ bits are transmitted creating an extra between-bit transition at $t_t + \frac{1}{2}\mathrm{T}_\mathrm{b}$. Note there is no between-bit transition between the ‘1 bit and the ‘0’ bit.

Assuming the decoder is already synchronised to valid transitions and starting from the beginning of a bit period the transition detector compares two consecutive samples to detect the transition at the centre of the bit period. Referring to Fig. 4, once a transition is detected at point A it is necessary to block any further transition for at least the next half bit period to avoid detection of between-bit transitions. This is done using a counter which is incremented at the sampling rate. The counter must also have finished its count in time so that the transition detector will detect the next valid transition

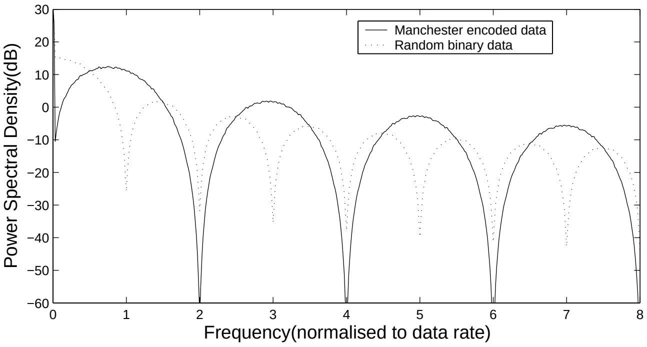

Fig. 3: Comparison of bandwidth of binary sequence and Manchester-encoded binary sequence.

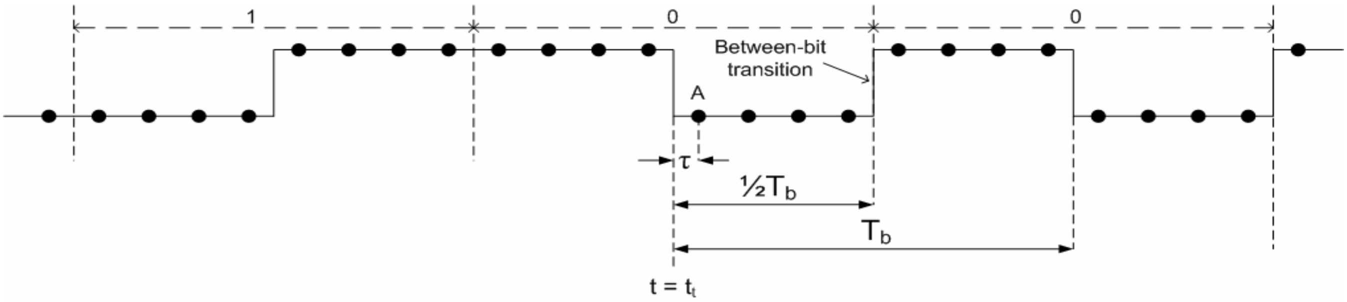

Fig. 4: An oversampled Manchester-encoded waveform formed from the bitstream "100".

at $t_t + \mathrm{T_b}$. Synchronisation to valid transitions occurs at any point when two consecutive bits have different values, therefore the preamble to a packet must contain at least one change in bit value.

Since the local sampling clock of the receiver is naturally not synchronised with the bit-clock of the transmitter it is required to take clock tolerances into account when designing the counter in the receiver.

The transition detector compares the current and previous samples when the counter is at zero, and therefore at the sample where the count returns to zero (when it counts for the *N*th time where *N* is the maximum count of the counter) it is possible to detect a transition. If a transition occurs at time t_t, and is detected at time $t_t + \tau$ (point A) (where $\tau = \alpha T_s$ and $0 \le \alpha < 1$), then the count $N-1$ must fall in the region between the invalid and valid transitions. Hence:

$$t_t + ½\mathrm{T_b} < t_t + \alpha T_s + (N-1)T_s < t_t + T_b \qquad (1)$$

Where T_s and T_b are the periods of the sampling and bitrate clocks respectively. Resolving and noting that $0 \le \alpha < 1$, the overall limits on the oversampling ratio ($R = T_b / T_s$) are:

$$N \le R < 2(N-1) \qquad (2)$$

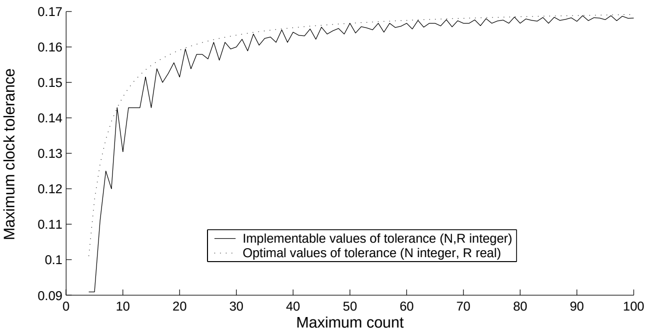

Fig. 5: Best achievable clock tolerance for increasing maximum count.

The permitted frequency tolerance for the DSP oscillators in the specks can be found by analysing the two worst cases of clock error, i.e. when the transmitter and receiver clocks are at either end of the specified oscillator frequency tolerance:

$$N[f_c \pm \delta f_c] \le R[f_c \mp \delta f_c] < 2(N-1)[f_c \pm \delta f_c] \qquad (3)$$

Where f_c and δ are the oscillator centre frequency and fractional tolerance respectively. Resolving the inequalities gives Equations 4a and 4b which express the bounds of permissible frequency error.

$$\delta_1(N,R) \le \frac{R-N}{R+N} \qquad (4a)$$

$$\delta_2(N,R) < \frac{2(N-1)-R}{2(N-1)+R} \qquad (4b)$$

The implementation of the decoder is therefore achieved by making a choice of the counter's maximum count, N, and the oversampling ratio to be used, R.

Fig. 5 shows the curve displaying the limit on clock tolerance ($R \in \mathbf{R}$ chosen to maximise tolerance), and the best implementable clock tolerance ($\{N,R\} \in \mathbf{Z}$) for varying values of N. This highlights that the tolerance will never rise above $\sqrt{2}-1/\sqrt{2}+1$. It should be noticed that the implemented values of N and R will always be integers, and as such the best tolerance is less likely to be achieved at realistic, low values of N and R. Fig. 6 shows the bounds of permissible frequency error for increasing values of R, as given by Equations (4a) and (4b). It can be seen that increasing R gives a better resolution of N and as such the peak tolerance where the bounds intersect can be approached more closely, an effect which is also seen in Fig. 5 as N increases. A practical implementation is realised by choosing a combination of N and R which approaches the intersection, as

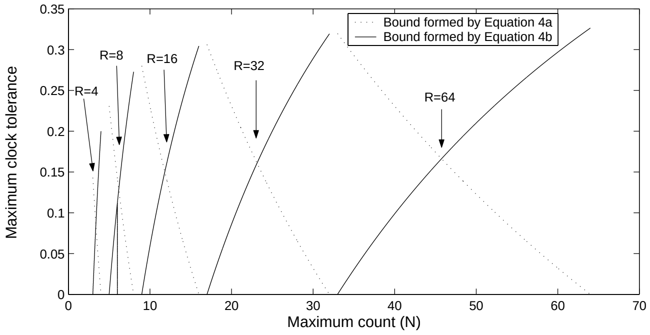

Fig. 6: Tolerance values for given values of maximum count and oversampling ratio.

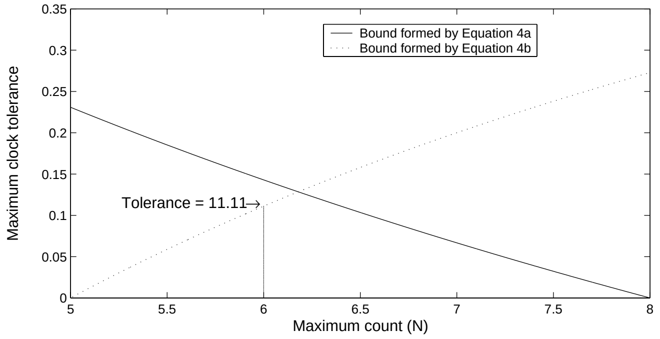

Fig. 7: A realistic implementation with oversampling ratio = 8 and maximum count = 6.

shown in Fig. 7 where using R = 8 and N = 6 gives a tolerance of 11.11%.

The decoder implementation of a transition detector and counter is therefore tolerant to a range of clock inaccuracies, and can be used to minimise power consumption through the use of an inaccurate, low-cost and low-power oscillator.

V. PULSE SHAPING

The previous analysis assumed an ideal, rectangular-shaped received signal. However, pulse shaping could alter the shape of the waveform presented to the bit-slicer. Pulse shaping for the Manchester encoded system has been considered in [6] where it is shown that it can affect the mark-to-space ratio of the input waveform to the decoder. Specifically half-sine shapes have been employed which can reduce the mark width. This effect is shown in Fig. 8. The mark width is reduced to between the times t_1 and t_2 in accordance with the level at which the threshold is set, where t_1 and t_2 are (for a half-sine pulse shape):

$$t_1 = \frac{\sin^{-1} V_T}{\pi} T_b \tag{5}$$

$$t_2 = T_b - \frac{\sin^{-1} V_T}{\pi} T_b \tag{6}$$

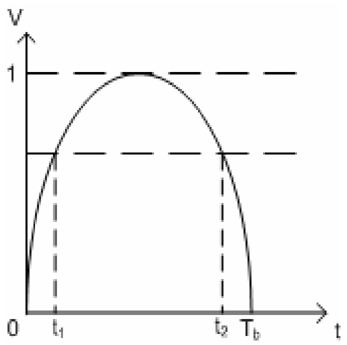

Fig. 8: Half-sine shaped pulse

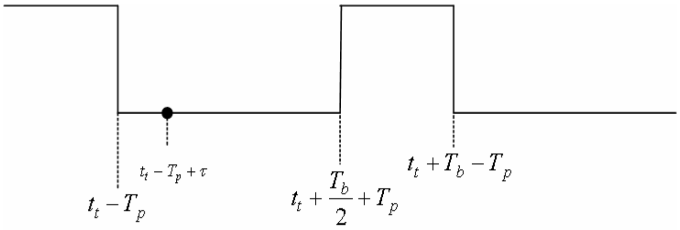

Fig. 9: Two successive pulse-shaped ‘0’ bits after slicing

And V_T is the threshold voltage. For analysis it is assumed that the signal is scaled between 0 and 1 and as such $0 \le V_T \le 1$.

The previous analysis can be performed on the waveform shown in Fig. 9 where again two successive ‘0’ bits are received. Note that the mark width is reduced according to V_T where:

$$T_P = \frac{\sin^{-1} V_T}{\pi} T_b \tag{7}$$

The result of reducing the mark width is that the upper limit on the oversampling ratio that can be used is reduced by a factor λ where:

$$\lambda = \frac{\pi}{\pi + 4\sin^{-1}(V_T)} \tag{8}$$

To ensure that the mark width is wide enough to allow operation of the decoder design the following condition on the threshold voltage applies:

$$0 \le V_T \le \sin\left(\pi\left(\frac{N-2}{4N}\right)\right) \tag{9}$$

The bounds on permissible frequency error for a half-sine shaped system are:

$$\delta_{1PS}(N,R)=\frac{R-N}{R+N} \qquad (10a)$$

$$\delta_{2PS}(N,R)=\frac{2\lambda(N-1)-R}{2\lambda(N-1)+R} \qquad (10b)$$

Fig. 10 shows the curve displaying the limit on clock tolerance ($R \in \mathbf{R}$ chosen to maximise tolerance), and the best implementable clock tolerance ($\{N,R\} \in \mathbf{Z}$) for varying values of N and λ highlighting that the tolerance will never rise above $\sqrt{2\lambda}-1/\sqrt{2\lambda}+1$. Table 1 shows some achievable tolerance values with N = 6.

TABLE 1:
ACHIEVABLE CLOCK TOLERANCES WITH N = 6 AND R CHOSEN TO MAXIMISE TOLERANCE.

Threshold Voltage	Tolerance (%)
0	11.11
0.1	7.69
0.2	6.41
0.3	1.44
≥ 0.4	0

VI. OSCILLATOR CONSIDERATIONS & FUTURE WORK

The clock oscillator on the speck will be an important consideration. At the current dimensions it will be possible to use a ceramic or crystal oscillator, however in future iterations it is believed that a bespoke silicon oscillator may be used.

A silicon oscillator would both allow device dimensions to be minimised and component costs and power consumption to be reduced. It may also have a wider specified frequency tolerance in which case the Manchester decoder design will be advantageous.

A further advantage of the Manchester system is that the decoder effectively ignores sample values while the counter is counting. It may be possible to switch off the analogue circuitry during these periods thus saving more power.

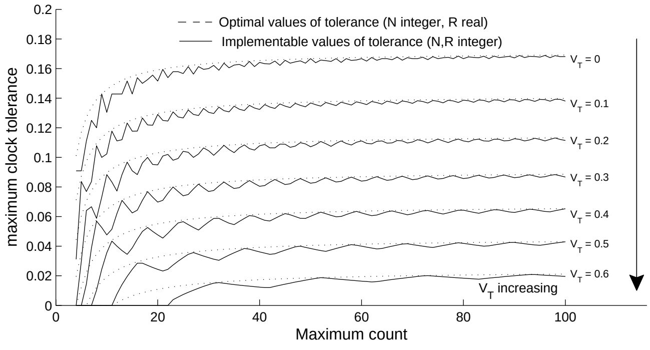

Fig. 10: Pulse-shaped system tolerance for varying values of maximum count.

The full performance characteristics of the Manchester system are still to be analysed. A performance and implementation cost comparison of the Manchester technique with commonly-used synchronisation techniques will be made. The effect of noise and channel effects on the signal presented to the analogue slicer and hence the Manchester decoder has also to be fully evaluated.

VII. CONCLUSIONS

Speckled computing is a new vision of wireless sensor networks that presents novel challenges to the design of a DSP physical layer. Power limitations necessitate that low-power consumption of the overall transceiver implementation is the priority design consideration. Under these constraints a Manchester-encoded transceiver has been implemented which trades bandwidth for design simplicity and low-power operation.

The design permits a low tolerance clock to be used. A realistic implementation using an oversampling ratio of 8 can provide a clock tolerance of more than 11%. By introducing half-sine pulse-shaping the clock tolerance value is reduced according to the value of the threshold voltage used to slice the received waveform.

ACKNOWLEDGEMENTS

This work is supported by the Scottish Higher Education Funding Council (SHEFC), and the Engineering and Physical Sciences Research Council (EPSRC).

The authors would like to thank members of the Speckled Computing Consortium for their input.

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